Syllabus and Course Information

ECE 2031 Digital Hardware Design, School of Electrical and Computer Engineering, 2 Credits

Lectures: 50 minutes a week , Labs: 2 hours 45 a week

Instructor Information

Instructor	Email	Drop-in Hours & Location
Dr. Simon Gautier	sgautier6@gatetch.edu	Typ. Wed. 9:30 11:30, Institut Lafayette Room 102

Teaching Assistant(s)	Email	Drop-in Hours & Location
		[N/A]
TBD		

General Information

This document provides logistical material for the Digital Design Laboratory and ECE 2031. Due dates for assignments are posted on Canvas.

The course will be fully on campus, subject to any changes in direction from campus leadership. The physical laboratory contains stations with a computer, prototyping units, oscilloscopes, and programmable logic development board. Attendance in lab (at the scheduled time) is required for all lab work, lab check-offs, and other activities.

Pre- &/or Co-Requisites

Either ECE 2020 or CS 2110 is a required prerequisite in digital logic theory, with a minimum grade of C. General programming experience and use of integrated development environments, such as from ECE 2035 or ECE 2036, is also required.

Course Goals and Learning Outcomes

The goal in ECE 2031 is to experience the conception, design, fabrication, and testing of digital hardware in a hands-on setting.

Laboratory projects will use a PC-based CAD tool environment that supports schematic capture, logic simulation, and VHDL-based logic synthesis on FPGAs (Field Programmable Gate Arrays). Discrete logic devices will be used for two designs, but VHDL-based logic synthesis on FPGA- based design boards will be used for more advanced design implementations. The semester will culminate with a design project specified and undertaken by teams of three students.

Technical communication skills are developed through laboratory reports, project documentation, and an oral presentation.

Course Objectives

As described at https://www.ece.gatech.edu/courses/course_outline/ECE2031, the objectives for students are to

1. apply their knowledge from ECE 2020 (or CS 2110) to practical laboratory experience in digital computing systems.
2. apply the concepts of basic combinational logic circuits, sequential circuit elements, and programmable logic in the laboratory setting.
3. develop familiarity and confidence with designing, building and testing digital circuits, including the use of CAD tools.
4. develop team-building skills and enhance technical knowledge through both written assignments and design projects.

Course Outcomes

Also from the ECE web site, upon successful completion of this course, students should be able to do the following:

- implement combinational logic circuits both with TTL devices on a protoboard and within a complex PLD.
- analyze the timing of digital circuits with oscilloscopes and logic analyzers.
- design and implement state machines to meet design specifications.
- design circuits with a graphical schematic CAD editor.
- simulate circuits within a CAD tool and compare to design specifications.
- design, implement, and simulate circuits using VHDL.
- implement a simple computer within a PLD.
- write machine language programs and assembly language programs for the simple computer.
- use a complex sequential logic circuit as part of a solution to an open-ended design problem.
- write laboratory reports and documentation conforming to technical writing standards.
- work effectively as team members to develop and write a group report.
- work effectively as team members to design an approved project.

Topics

The primary topics of the course include

- CAD Tools
- Combinational logic design using multiple methods: discrete logic devices, schematic capture for FPGAs, and VHDL
- Examination of real timing issues on hardware using software simulation and hardware test equipment (oscilloscope)
- State machine specification, design, simulation, and implementation with multiple methods

- VHDL models of basic gates and logic operations
- Logic synthesis and simulation using VHDL
- Design verification with a logic analyzer
- VHDL models of data storage elements
- ROM and RAM implementations on an FPGA board
- Hardware design of a simple computer with ALU, registers, control unit, memory, instructions, and I/O
- VHDL-based simple computer simulation and implementation on FPGA board
- Machine language and assembly language programming for the simple computer
- Simulation and implementation of programs on the FPGA board
- Final design project problem specification (examples: video game, control application, robot, or contest)
- Hardware and tools available to solve the final design project problem
- Project engineering issues: top-down vs. bottom-up design, hierarchical decomposition, and modularity

The learning outcomes for this course are proficiency in all of the topics listed above.

The ECE Undergraduate Professional Communication Program (UPCP), often called the "Writing Program," is integrated with ECE 2031. This will be the first of several courses in ECE in which you are instructed in techniques for presenting technical information. CS and other majors taking ECE2031 have the same technical communication requirements and get the same advice and consultation on written and oral communication skills.

Course Requirements & Grading

The course grade is determined according to the following weights:

- 25 % Lab reports
- 25% Prelab quizzes
- 10 % One or more Lab Practical Exercises
- 20 % Final Project
- 20 % In-class Exam

The written exams are closed book and closed note. The lab practical exam is open book, open notes. The lab practical exam will be determined later in the semester. At the beginning of all exams, any electronic communication device must be turned off and put away for the duration of the exam.

All grades will be recorded on Canvas. Your uncurved calculation is the best indicator of your grade. With the contribution of "easy" points like participation and asynchronous quizzes, and an exam score that will already be curved as needed, there is no need to adjust the final grades.

There is no exam during finals week. The project replaces the final exam, and some of the project-related assignments are due on the final instructional days of the semester.

The in-class exam will be taken during lecture time unless otherwise arranged due to time conflicts or other issues.

Lab quizzes will be given for each of the eight labs, and early in the project. The quizzes are proctored assessments, and together form the equivalent length of an exam and carry a similar weight. Each quiz is focused on the current background reading and prelab exercises, recent asynchronous material, and the most recent lecture, but can also be related to earlier course information and lab work. They must be taken at the start of the relevant lab session, in the laboratory.

The lowest lab quiz score will be dropped. Each quiz will contribute approximately the same amount to the total quiz category, but the number of points that each quiz contributes might vary, and Canvas will drop the quiz with the lowest individual percentage score.

Online asynchronous quizzes associated with asynchronous learning activities will be given multiple times during the semester, related to some material that students are supposed to view outside of class, usually prior to a related lecture or lab. The deadlines for online quizzes will be shown on each one on Canvas.

Extra Credit Opportunities

Offering a higher grade for additional work is not fair to students with a tight schedule, so there are no opportunities for extra credit in this class. There are many opportunities to get perfect scores simply by participating and being on time. These are the rewards to students who are diligent throughout the semester.

Grading Scale

Your final grade will be assigned as a letter grade according to the following scale:

A	90-100%
B	80-89%
C	70-79%
D	60-69%
F	0-59%

According to policy, grades at Georgia Tech are interpreted as follows:

A	Excellent (4 quality points per credit hour)
B	Good (3 quality points per credit hour)
C	Satisfactory (2 quality points per credit hour)
D	Passing (1 quality point per credit hour)
F	Failure (0 quality points per credit hour)

See http://registrar.gatech.edu/info/grading-system for more information about the grading system at Georgia Tech.

Course Materials

Course Text

There are no required textbooks for this course. The previous printed lab manual (*Digital Design Laboratory Manual, Second Edition*, by Thomas R. Collins and Christopher Twigg) has been revised, and derived material is being made available electronically.

In previous semesters, some reading assignments were made in *Rapid Prototyping of Digital Systems*, by J. O. Hamblen, T. S. Hall, and M. D. Furman ("SOPC Edition"). There will be no assignments made in that book this semester. But for anyone who seeks additional background, an electronic version is available online through the Georgia Tech library website.

For any students who desire additional prerequisite logic course coverage, a recommended textbook is Harris and Harris, *Digital Design and Computer Architecture*. No assignments will be made in this textbook, but students often ask for suggestions, and this not only covers the core aspects from the prerequisite, but also provides some additional coverage of VHDL, which will be covered in this course, and it is available for free through the library.

Course Website and Other Classroom Management Tools

The link to the class room website is https://powersof2.gatech.edu/labmanual. Labs will be posted on a weekly basis. It is Students responsability to check this link for updates.

In addition to the online materials, you will need to have the following:

Hardware:
o A reliable home computer, meeting the requirements described in Lab0 available at the start of the semester.
o No board nor small parts are required, all parts are provided by GTE

Your personal GT computer account, which is needed to access Canvas and other portals that are protected by Georgia Tech single sign-on login, and a reliable means of two- factor authentication for that login.

FPGA development boards (the DE10-Standard) are installed in the lab, and hardware-related work must be done there. As will be described, "pre-lab" work will be done at home and does not require the lab hardware.

Your personal computer should be available for you to install software during the first week of class. The personal hardware items described above are needed for the second lab, done in the third week of classes (see the schedule on Canvas).

Everyone should maintain backups of all work with institute-provided resources like PRISM or OneDrive or by any other means, preferably at a location other than their computer. However, the CAD software has been known to have errors when compiling from a network or cloud drive. Even on campus, it is **5-10 times slower when you compile files from a remote location (which includes your desktop) or from a flash drive.** So,

it is wise to keep your active project work on the local hard drive and make backups regularly to avoid late penalties if something is lost without easy restoration.

Academic Integrity

Georgia Tech aims to cultivate a community based on trust, academic integrity, and honor. Students are expected to act according to the highest ethical standards. For information on Georgia Tech's Academic Honor Code, please visit http://www.catalog.gatech.edu/policies/honor-code/ or http://www.catalog.gatech.edu/rules/18/.

Any student suspected of cheating or plagiarizing on a quiz, exam, or assignment will be reported to the Office of Student Integrity, who will investigate the incident and identify the appropriate penalty for violations.

Accommodations for Students with Disabilities

If you are a student with learning needs that require special accommodation, contact the Office of Disability Services at (404)894-2563 or http://disabilityservices.gatech.edu/, as soon as possible, to make an appointment to discuss your special needs and to obtain an accommodations letter. Please also e-mail me as soon as possible in order to set up a time to discuss your learning needs.

Also, note that accommodations are given per assignment. As an exam approaches, for example, where accommodations are needed, you must request accommodations (similar to what you would do on campus, requesting use of the Testing Center). Merely having discussed accommodations at the start of the semester is not sufficient.

Attendance and/or Participation

Lab Attendance Policy

All students are required to attend their assigned lab section beginning the second week of classes. Students may *also* use other lab sections as open hours if there is space and when an activity is not taking place (most notably lab quizzes and practical exercises).

Lecture Attendance Policy

The lectures will be in person. Recordings will be made available, but only for the purpose of later reference.

Excused Absences

When a student has a valid excuse for missing a lecture, they should communicate it via Canvas, in the participation assignment related to the relevant lecture. If the excuse is acceptable, the assignment will be marked as "excused," which removes it from the grade calculation.

For excused absences affecting other work and falling under institute guidelines (school function, illness, injury, etc.; see http://www.catalog.gatech.edu/rules/4/), at the earliest opportunity, Dr. Gautier and your GTA should be contacted. In particular, the instructor should be contacted about making up assessments (tests, practical exercises, etc.), and your GTA should be contacted about lab-related work (lab reports, writing assignments, lab quizzes, etc.).

For circumstances not covered by institute policy (job interviews, transportation problems, personal crises, etc.), contact the instructor as soon as the situation is known. If it is deemed excusable, appropriate (perhaps partial) accommodations will be made.

Unexcused Missed Exams

In general, an unexcused missed exam will result in a grade of zero, or the curved equivalent of a zero (if a curve applies). However, it would be to the advantage of a student to discuss a missed exam at the first opportunity with Dr. Gautier.

Unexcused Missed Practical Exercises

Practical exercises take place at the beginning of the lab section at two specific times in the semester shown in the class schedule. Students who miss the exercise will be given the opportunity to make it up in a later section or other time within one week with a 15% penalty.

Unexcused Late Lab Work

Completion of lab steps is recorded via check-offs, which are earned by showing or demonstrating the result of specific lab steps to a UTA. Credit for the check-offs is included as part of the lab report grade.

There are two categories of check-offs: those associated with prelab work, and those associated with in-lab work. Prelab work is intended to be completed before coming to lab, and prelab check-offs are due by the end of the first hour in the associated lab session (the hour is to allow you to take the quiz first and for TAs to get the check-offs done). Lab check-offs are due by close-of-lab on the following day; e.g. if your lab session is on Tuesday, lab check-offs are due when the lab closes on Wednesday.

After those soft deadlines, check-offs may be completed late with a 15% penalty (applied per check-off, and flat, not per-day) until the hard deadline, which depends on your lab section:

- Monday & Tuesday lab sections: end of open hours the following weekend.
- Wednesday lab sections: close-of-lab the following Monday.
- Thursday lab sections: close-of-lab the following Tuesday.

The exact lab schedule (which determines when close-of-lab is for any particular day) depends on when TAs are available, and so cannot be created until after the first week of classes. Once created, it will be available on Canvas, linked from the syllabus page.

Student-Faculty Expectations Agreement

At Georgia Tech we believe that it is important to strive for an atmosphere of mutual respect, acknowledgement, and responsibility between faculty members and the student body. See http://www.catalog.gatech.edu/rules/22/ for an articulation of some basic expectation that you can have of me and that I have of you. In the end, simple respect for knowledge, hard work, and cordial interactions will help build the environment we seek. Therefore, I encourage you to remain committed to the ideals of Georgia Tech while in this class.

Course Schedule (tentative, subject to small adjustments)

Date	Lecture Topic	Lab Topic
Week 1	Introduction	No lab
Week 2	Computer Aided Logic Design	Lab 1
Week 3	Discrete Circuits	Lab 2
Week 4	Circuit Characteristics	Lab 3
Week 5	State Machines (SMs) and VHDL I (written exam)	Lab 4
Week 6	VHDL II and Sequential Timing	Lab 5
Week 7	Train Lab	Lab 6
Week 8	Simple Computer I	Lab 7
Week 9	Simple Computer II	Lab 8
Week 10	Practical Exam Review	Practical Exam
Week 11	Project Proposal	Project
Week 12	Written Exam	Design Summary
Week 13&14	Presentation & Report Tips	Project/Demos