Syllabus: ECE 2031 Digital Hardware Design

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Teaching Assistant(s): TBD

General Information: Due dates for assignments will be posted on Canvas. The physical laboratory contains stations with a computer, prototyping units, oscilloscopes, and programmable logic development board. Attendance in lab (at the scheduled time) is required for all lab work, lab check-offs, and other activities. Pre- &/or Co-Requisites Either ECE 2020 or CS 2110 is a required prerequisite in digital logic theory. General programming experience and use of integrated development environments, such as from ECE 2035 or ECE 2036, is also required.

Course Goals and Objectives: Laboratory projects will use a PC-based CAD tool environment that supports schematic capture, logic simulation, and VHDL-based logic synthesis on FPGAs (Field Programmable Gate Arrays). Discrete logic devices will be used for two designs, but VHDL-based logic synthesis on FPGA- based design boards will be used for more advanced design implementations. The semester will culminate with a design project specified and undertaken by teams of students. Technical communication skills are developed through laboratory reports, project documentation, and an oral presentation.

The objectives for students are to:

1. Apply their knowledge from ECE 2020 (or CS 2110) to practical laboratory experience in digital computing systems.
2. Apply the concepts of basic combinational logic circuits, sequential circuit elements, and programmable logic in the laboratory setting.
3. Develop familiarity and confidence with designing, building and testing digital circuits, including the use of CAD tools.
4. Develop team-building skills and enhance technical knowledge through both written assignments and design projects.

Course Outcomes:

1. implement combinational logic circuits both with TTL devices on a protoboard and within a complex PLD.
2. Analyze the timing of digital circuits with oscilloscopes and logic analyzers.
3. Design and implement state machines to meet design specifications.
4. Design circuits with a graphical schematic CAD editor.
5. Simulate circuits within a CAD tool and compare to design specifications.
6. Design, implement, and simulate circuits using VHDL.
7. Implement a simple computer within a PLD.

8. Write machine language programs and assembly language programs for the simple computer.
9. Use a complex sequential logic circuit as part of a solution to an open-ended design problem.
10. Write laboratory reports and documentation conforming to technical writing standards.
11. Work effectively as team members to develop and write a group report.

Topics:

1. CAD Tools
2. Combinational logic design using multiple methods: discrete logic devices, schematic capture for FPGAs, and VHDL
3. Examination of real timing issues on hardware using software simulation and hardware test equipment (oscilloscope)
4. State machine specification, design, simulation, and implementation with multiple methods
5. VHDL models of basic gates and logic operations
6. Logic synthesis and simulation using VHDL
7. Design verification with a logic analyzer
8. VHDL models of data storage elements
9. ROM and RAM implementations on an FPGA board
10. Hardware design of a simple computer with ALU, registers, control unit, memory, instructions, and I/O
11. VHDL-based simple computer simulation and implementation on FPGA board
12. Machine language and assembly language programming for the simple computer
13. Simulation and implementation of programs on the FPGA board
14. Final design project problem specification (examples: video game, control application, robot, or contest)
15. Hardware and tools available to solve the final design project problem
16. Project engineering issues: top-down vs. bottom-up design, hierarchical decomposition, and modularity

Required Books and Materials:

There are no required textbooks for this course. The previous printed lab manual (Digital Design Laboratory Manual, Second Edition, by Thomas R. Collins and Christopher Twigg) has been revised, and derived material is being made available electronically. In previous semesters, some reading assignments were made in Rapid Prototyping of Digital Systems, by J. O. Hamblen, T. S. Hall, and M. D. Furman ("SOPC Edition"). There will be no assignments made in that book this semester. But for anyone who seeks additional background, an electronic version is available

online through the Georgia Tech library website. For any students who desire additional prerequisite logic course coverage, a recommended textbook is Harris and Harris, Digital Design and Computer Architecture. No assignments will be made in this textbook, but students often ask for suggestions, and this not only covers the core aspects from the prerequisite, but also provides some additional coverage of VHDL, which will be covered in this course, and it is available for free through the library. 5 In addition to the online materials, you will need to have the following:

Hardware:

- A reliable home computer, meeting the requirements described in Lab 0 available at the start of the semester.
- A kit of integrated circuits (logic chips), wires, a protoboard (breadboard), and other small electronic parts.

Your personal GT computer account, which is needed to access Canvas and other portals that are protected by Georgia Tech single sign-on login, and a reliable means of two-factor authentication for that login. FPGA development boards (the DE10-Standard) are installed in the lab, and hardware-related work must be done there. As will be described, “pre-lab” work will be done at home and does not require the lab hardware. Your personal computer should be available for you to install software during the first week of class. The personal hardware items described above are needed for the second lab, done in the third week of classes (see the schedule on Canvas). Everyone should maintain backups of all work with institute-provided resources like PRISM or OneDrive or by any other means, preferably at a location other than their computer. However, the CAD software has been known to have errors when compiling from a network or cloud drive. Even on campus, it is 5-10 times slower when you compile files from a remote location (which includes your desktop) or from a flash drive. So, it is wise to keep your active project work on the local hard drive and make backups regularly to avoid late penalties if something is lost without easy restoration.

Communication:

We will utilize Canvas as the primary means of navigating the course using the Modules page. You may have already viewed some Canvas content, including announcements. If not, go to http://canvas.gatech.edu, log in with your Tech credentials, and you should see ECE 2031 as one of your courses.

Grading:

20% synchronous exam

10% two practical exercises

20% lab quizzes (8 total quizzes, with the lowest score dropped)

5% class participation, mainly consisting of completing surveys and other online tasks, attending lecture, participating in class activities, such as breakout groups and discussions

25% eight structured labs, including technical credit for completion (recorded by check-offs) and for accurate description of results, and communication credit for clear and effective presentation of required results.

20% prepared work related to design project – 1300 total points broken up into: Proposal Presentation (400 points), Design logbook (50 points), Project demonstration (500 points), Project files (50 points), Design Summary (300 points)

There is no exam during finals week. The project replaces the final exam, and some of the project-related assignments are due on the final instructional days of the semester.